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# SCT1180



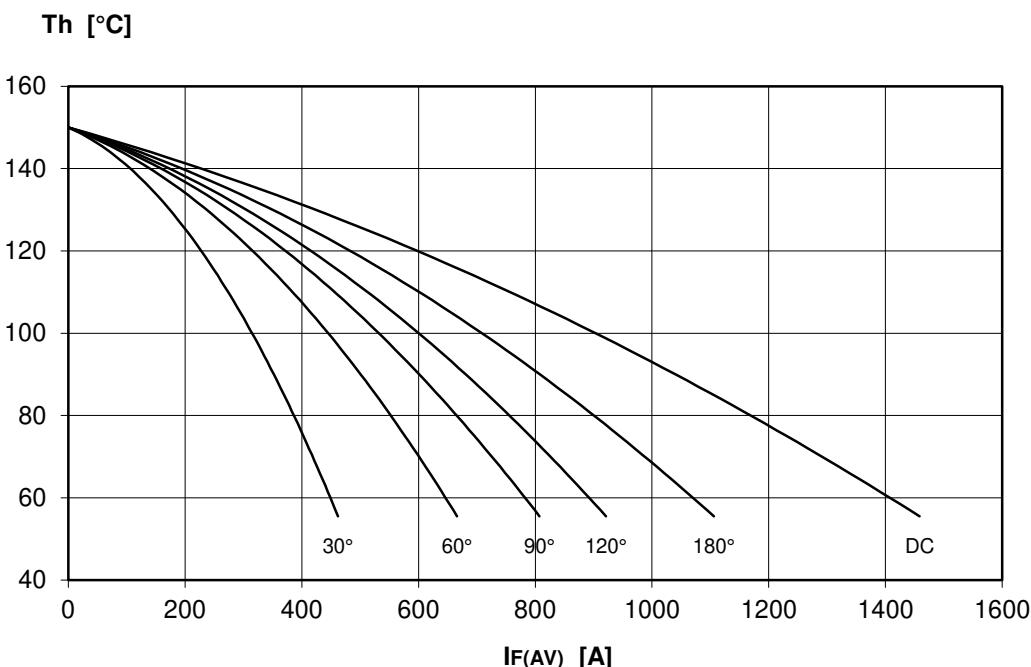
## Power Rectifier Diodes

Repetitive voltage up to	<b>800 V</b>
Mean forward current	<b>1102 A</b>
Surge current	<b>12 kA</b>

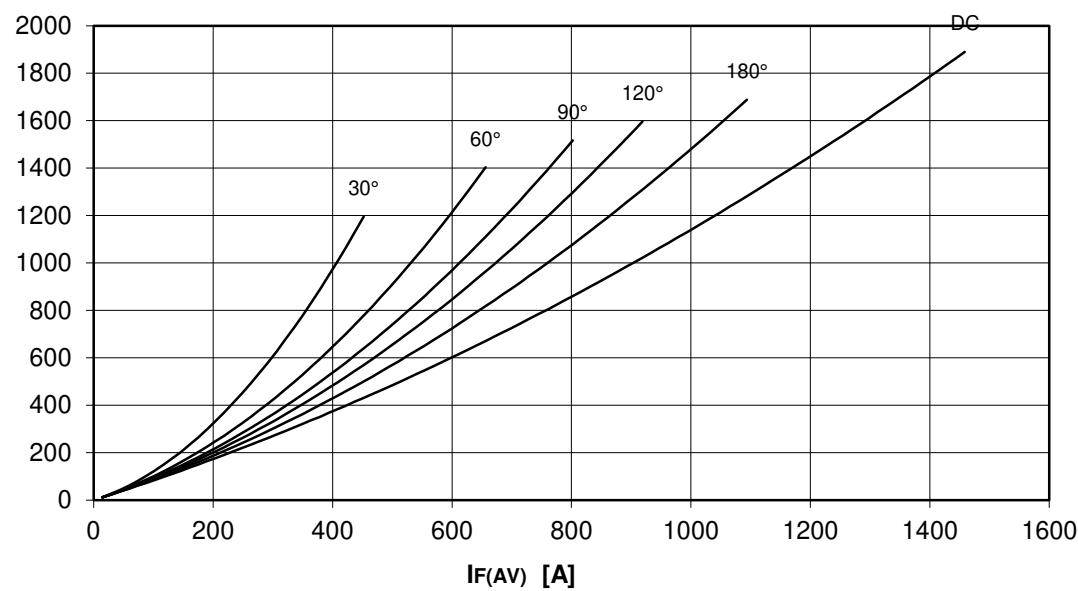
Symbol	Characteristic	Conditions	T <sub>j</sub> [°C]	Value	Unit
<b>BLOCKING</b>					
V <sub>RRM</sub>	Repetitive peak reverse voltage		150	800	V
V <sub>RSM</sub>	Non-repetitive peak reverse voltage		150	900	V
V <sub>DRM</sub>	Repetitive peak off-state voltage		150	800	V
I <sub>RRM</sub>	Repetitive peak reverse current	V=V <sub>RRM</sub>	150	50	mA
I <sub>DRM</sub>	Repetitive peak off-state current	V=V <sub>DRM</sub>	150	50	mA
<b>CONDUCTING</b>					
I <sub>T(AV)</sub>	Mean forward current	180° sin, 50 Hz, Th=55°C, double side cooled		1102	A
I <sub>T(AV)</sub>	Mean forward current	180° sin, 50 Hz, Tc=85°C, double side cooled		1086	A
I <sub>TSM</sub>	Surge forward current	Sine wave, 10 ms without reverse voltage	150	12	kA
I <sup>2</sup> t	I <sup>2</sup> t			720 × 10 <sup>3</sup>	A <sup>2</sup> s
V <sub>T</sub>	On-state voltage	On-state current = 1900 A	25	1,45	V
V <sub>T(TO)</sub>	Threshold voltage		150	0,80	V
r <sub>T</sub>	On-state slope resistance		150	0,340	mohm
<b>SWITCHING</b>					
di/dt	Critical rate of rise of on-state current, min.	From 75% V <sub>DRM</sub> up to 1200 A; gate 10V, 5Ω	150	200	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of V <sub>DRM</sub>	150	500	V/μs
t <sub>d</sub>	Gate controlled delay time, typical	V <sub>D</sub> =200V; gate source 20V, 10Ω, tr=.5 μs	25	1,5	μs
t <sub>q</sub>	Circuit commutated turn-off time, typical	dv/dt = 20 V/μs linear up to 80% V <sub>DRM</sub> di/dt = -20 A/μs, I= 1000 A			μs
Q <sub>rr</sub>	Reverse recovery charge		150		μC
I <sub>rr</sub>	Peak reverse recovery current	VR= 50 V			A
I <sub>H</sub>	Holding current, typical	V <sub>D</sub> =5V, gate open circuit	25	300	mA
I <sub>L</sub>	Latching current, typical	V <sub>D</sub> =5V, tp=30μs	25		mA
<b>GATE</b>					
V <sub>GT</sub>	Gate trigger voltage	V <sub>D</sub> =5V	25	3,50	V
I <sub>GT</sub>	Gate trigger current	V <sub>D</sub> =5V	25	200	mA
V <sub>GD</sub>	Non-trigger gate voltage, min.	V <sub>D</sub> =V <sub>DRM</sub>	150	0,25	V
V <sub>FGM</sub>	Peak gate voltage (forward)			30	V
I <sub>FGM</sub>	Peak gate current			10	A
V <sub>RGM</sub>	Peak gate voltage (reverse)			5	V
P <sub>GM</sub>	Peak gate power dissipation	Pulse width 100 μs		150	W
P <sub>G</sub>	Average gate power dissipation			2	W
<b>MOUNTING</b>					
R <sub>th(j-h)</sub>	Thermal impedance, DC	Junction to heatsink, double side cooled		50,0	°C/kW
R <sub>th(c-h)</sub>	Thermal impedance	Case to heatsink, double side cooled		15,0	°C/kW
T <sub>j</sub>	Operating junction temperature			-30 / 150	°C
F	Mounting force			8,0 / 9,0	kN
	Mass			85	g

## DISSIPATION CHARACTERISTICS

SQUARE WAVE

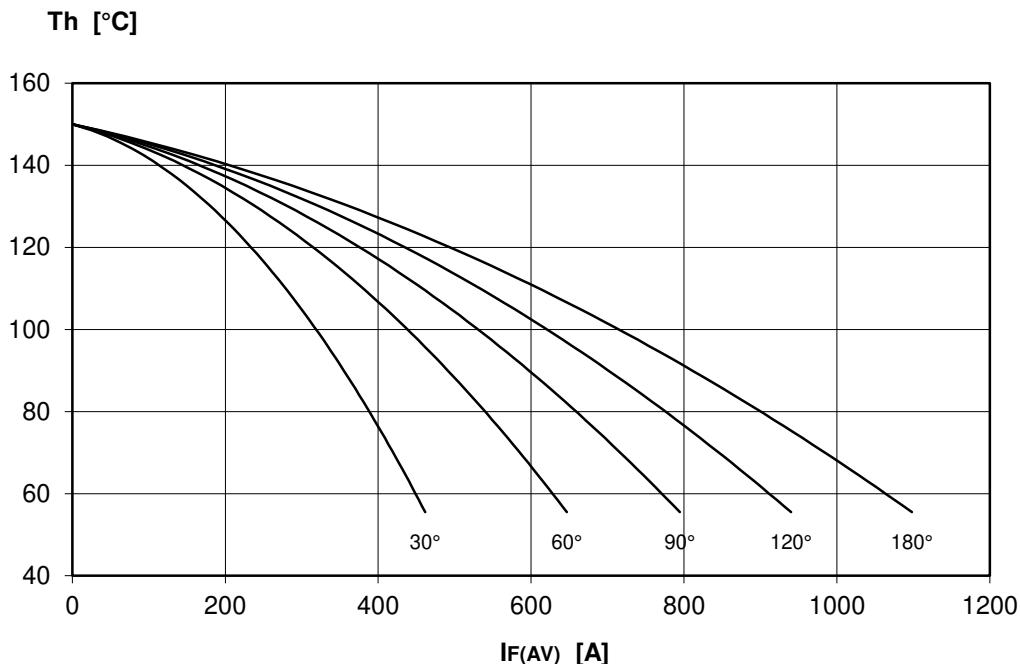


PF(AV) [W]

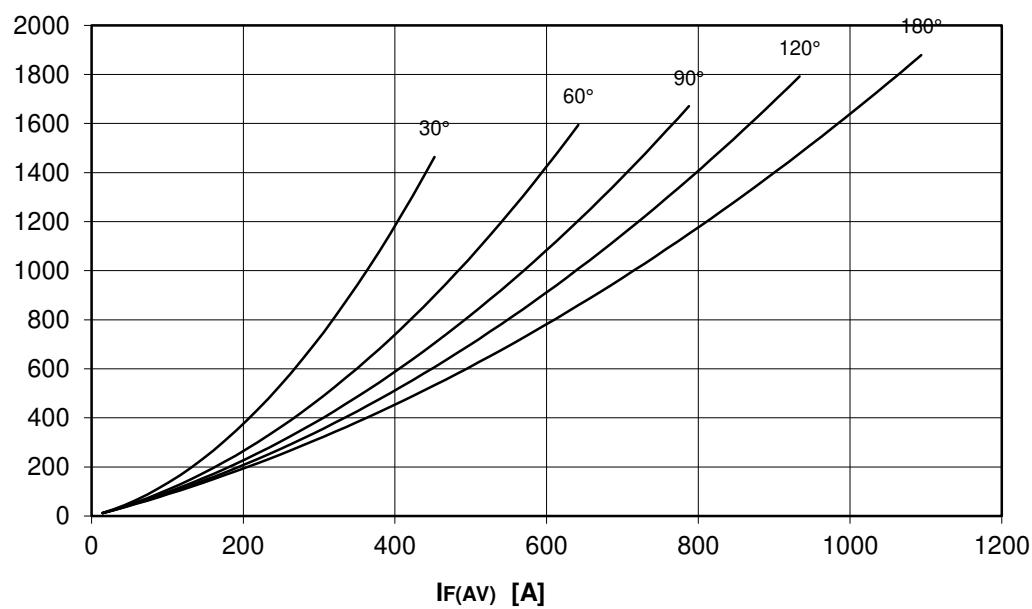


## DISSIPATION CHARACTERISTICS

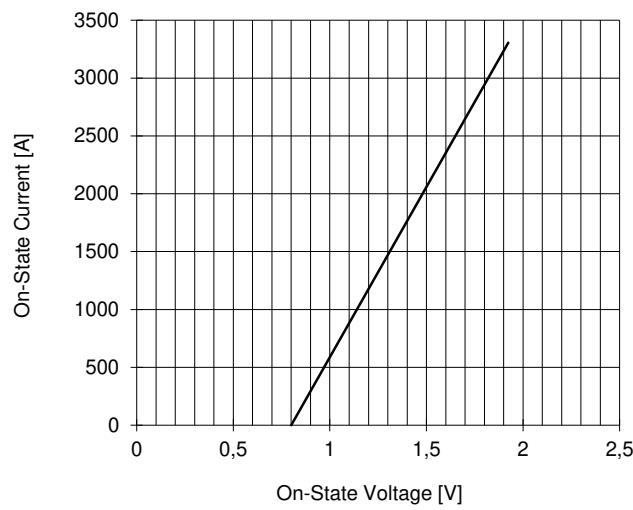
SINE WAVE



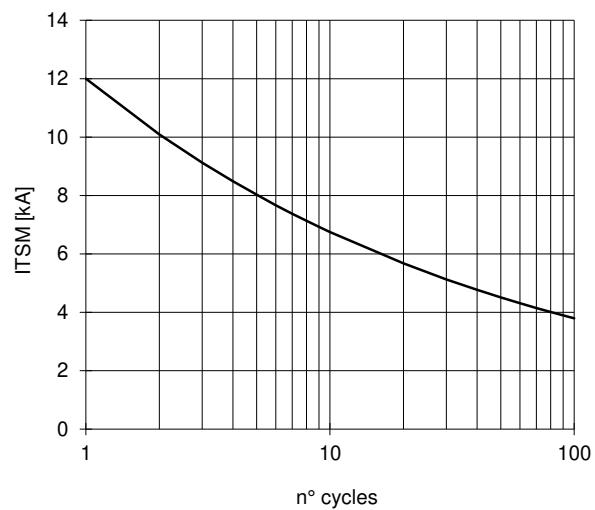
PF(AV) [W]



ON-STATE CHARACTERISTIC  
 $T_j = 150 \text{ }^{\circ}\text{C}$



SURGE CHARACTERISTIC  
 $T_j = 150 \text{ }^{\circ}\text{C}$



TRANSIENT THERMAL IMPEDANCE  
 DOUBLE SIDE COOLED

